

Capacitors

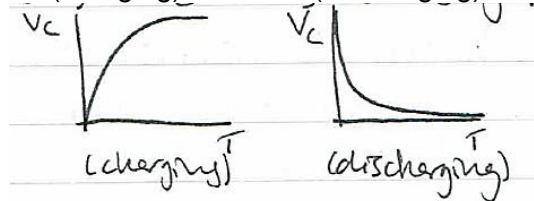
- are capable of storing electrical charge and energy
- will block DC but allow AC to pass
- in parallel, act like resistors in series, whereas in series act like resistors in parallel

Resistor–Capacitor Networks

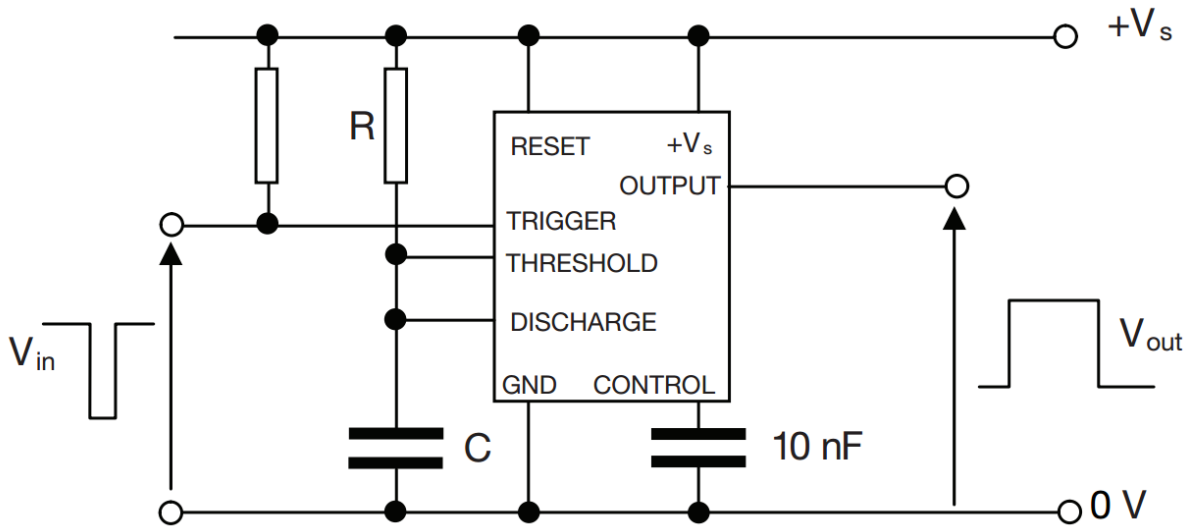
- the time constant is the time taken for a capacitor to charge/discharge by 63% of its maximum

$$T = R \times C$$

- after  $1T$ ,  $V_C = 0.63V_S$  (charging), or  $V_C = 0.37V_S$  (discharging)
- after  $0.69T$ ,  $V_C = 0.5V_S$
- after  $5T$ ,  $V_C = V_S$  (charging) or  $V_C = 0$  (discharging)



Timing systems: The Monostable



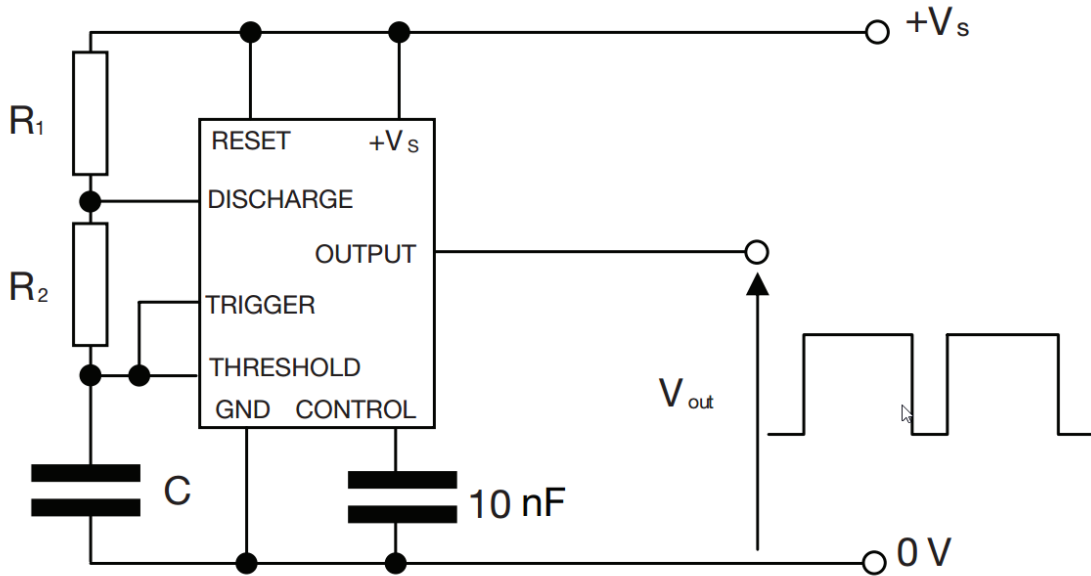
Note that **THRESHOLD and DISCHARGE** are connected to each other

The 555 monostable has a stable and unstable output state.

1. triggered by  $V_{IN}$  falling below  $1/3 V_S$  momentarily (falling edge)
2. capacitor  $C$  begins to charge through  $R$ , and output =  $V_S$
3. output =  $V_S$  until  $V_C > 2/3 V_S$  ('threshold switching voltage'). At this point, output = 0
4.  $V_C > 2/3 V_S$ , output = 0 & DISCHARGE connects to 0V, quickly discharging  $C$

The time period of a monostable is given by  $T = 1.1RC$

Timing systems: The Astable



Note that **TRIGGER** and **THRESHOLD** are connected.

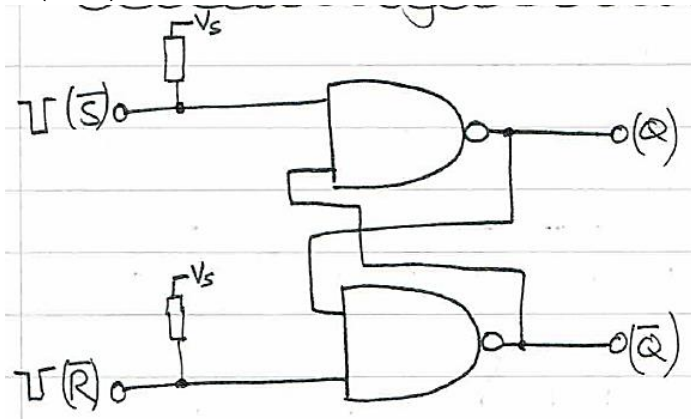
An astable has no stable output state but constantly changes.

1. initially C discharged, so  $V_C < V_{TRIG}$  ( $1/3 V_S$ ) thus output =  $V_S$
  2. C charges through  $R_1 + R_2$  until  $V_C > V_{THRESH}$  ( $2/3 V_S$ ), at which point output = 0, and discharge connects to 0V
  3. C now discharges through  $R_2$  until  $V_C < V_{TRIG}$ . At this point output =  $V_S$  and the process repeats
- Note first pulse longer than the rest as C has to charge from 0V rather than  $1/3 V_S$

The AQA GCE Electronics datasheet gives equations for  $T_H$ ,  $T_L$  and  $f$ . Time period =  $T_H + T_L$ , or  $1/f$ .

SEQUENTIAL LOGIC SYSTEMS

The NAND-gate bistable (latch)

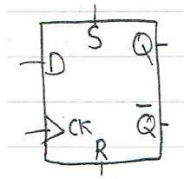


Assuming  $Q=0$  and  $\bar{Q}=1$ , when a short pulse to 0V is applied to SET,  $Q=1$  &  $\bar{Q}=0$ . If a short 0V pulse is now applied to RESET,  $Q=0$  and  $\bar{Q}=1$  (the initial state).

The two resistors 'pull up' the inputs to  $V_S$  to allow for the 0V pulses. When working through the system, start from the input of the new pulse and follow through.

### D-type flip-flop

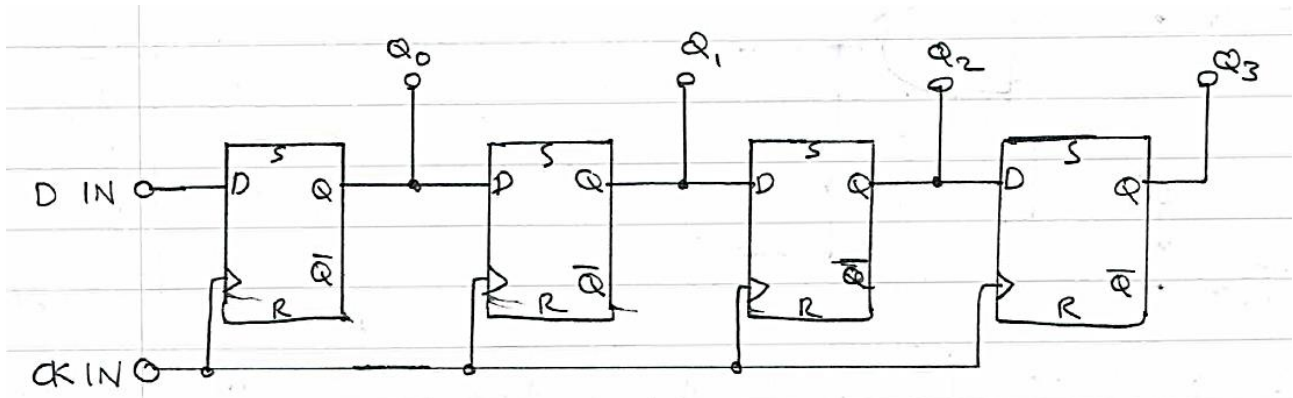
One cannot synchronise several NAND-gate bistables together. The NAND-gate bistable also has an unstable state where  $S$  &  $R = 0$ . The Data-type flip-flop overcomes these issues.



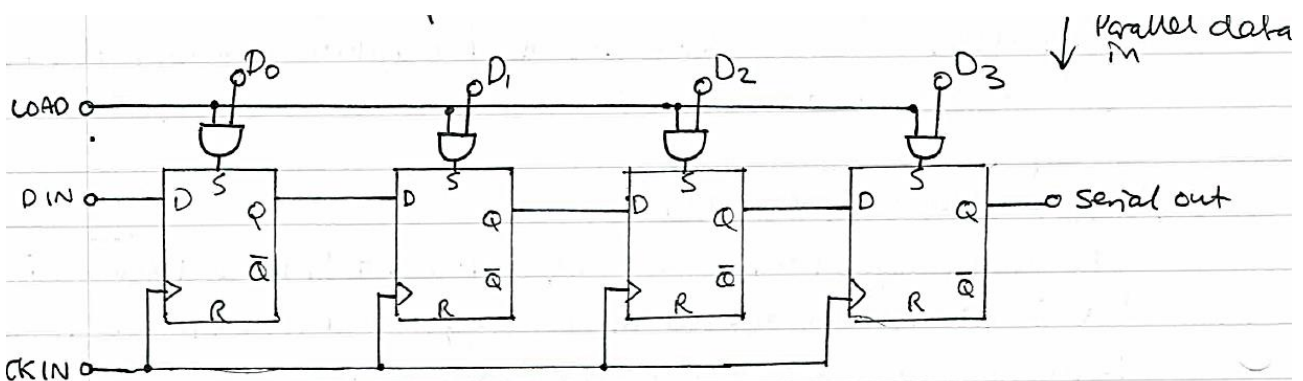
- on rising edge at clock, data at D is copied to Q
- alternatively a pulse at SET will make Q a logic 1, regardless of the condition of D and CK
- a pulse at RESET similarly will make Q a logic 0.

### SHIFT REGISTERS

- enable data to be passed from one flip-flop to the next on each successive clock pulse



The above is a **SIPO**. Series data goes in, and parallel data comes out on the  $Q_n$  outputs. The data moves along with each successive clock pulse.

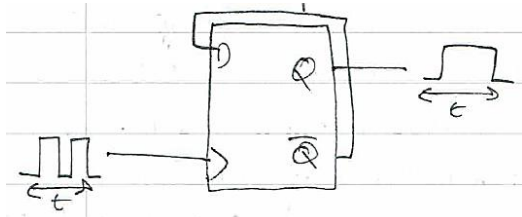


The above is a **PISO**. Parallel In Serial Out. Data arrives at  $D_n$  and is loaded via 'LOAD', and can then be shifted along and out the end by clock pulses.

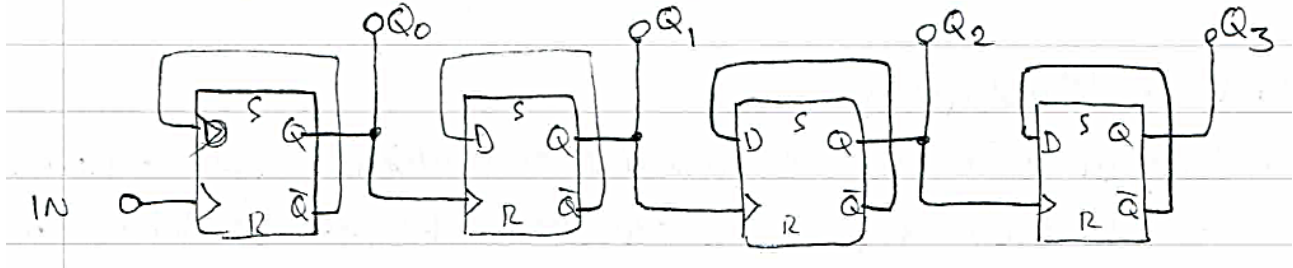
One application of a large shift register is to generate a pseudorandom number by X-ORing two of the outputs into the data input.

## COUNTER SUBSYSTEMS

### divide-by-two frequency counter

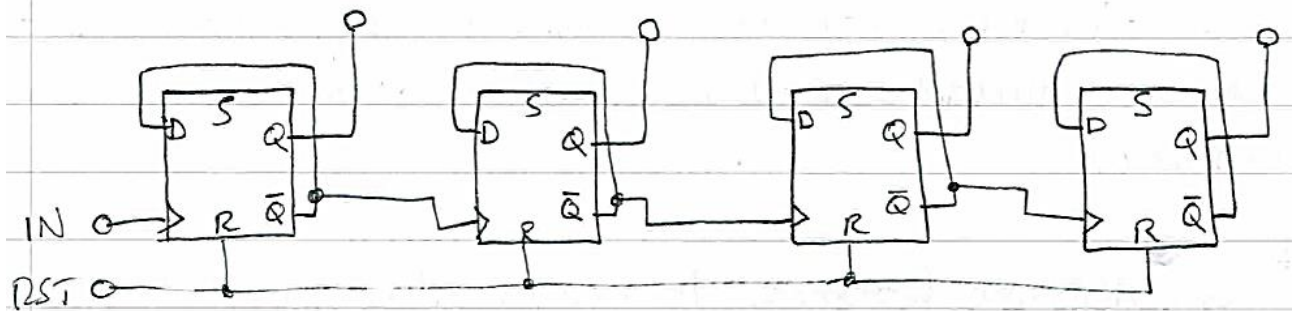


### 4-bit DOWN counter



The above circuit counts down from 15 to 0 and will also act as a frequency divider.

### 4-bit UP counter



This circuit counts up from 0 to 15.

With either counter, we can shorten the count by looking at the binary output and AND-gating together the necessary outputs (eg look for where two 1s appear only at the same time) into a 'RESET' rail.

Note – we will not get an even mark:space ratio using these systems unless the final flip-flop is acting as a divide-by-two counter.

The number of pulses required to return the system to its initial state is known as the '**modulo**'.

### Using a 7-seg display with binary coded decimal (BCD) & hex counters

There are ICs available to decode binary, BCD, or hex, and operate a 7-seg. eg 4511. The 4026 also contains a decade counter.

## OPERATIONAL AMPLIFIERS

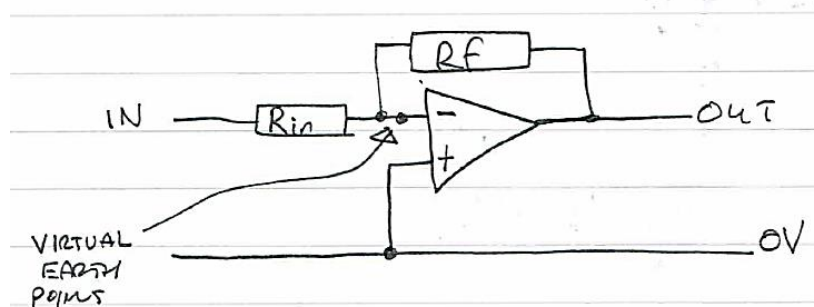
- recall the basic properties from ELEC1:
  - ideal op-amp has: very large  $A_{OL}$  (reality, only at low freqs); maximum output equal to  $V_S$  (reality, usually 2V less); infinite input impedance so no current passes into the input terminals (reality, few nA); zero output impedance so can supply any required current (reality; only a few mA);  $V_{OUT}=0$  when inputs equal (reality, small offset).

### Gain and bandwidth

- bandwidth: the “range of frequencies over which the power gain is at least half the maximum”, or “voltage gain at least 70% ( $\frac{\sqrt{2}}{2}$ ) of the maximum”
- the open loop voltage gain ( $A_{OL}$ ) decreases with frequency – can be plotted as a straight line logarithmic graph
- *voltage gain*  $\times$  *bandwidth* = *gain bandwidth product*
- using frequency compensated op-amps it is not possible to have a single op-amp with both large voltage gain and large bandwidth – we need to cascade multiple op-amps together, remembering that the gains are multiplied (eg two op-amps with gain 3 give a total gain 9)
- negative feedback is used to reduce the overall voltage gain of a system as it drives the inputs together.

## AMPLIFIER SUBSYSTEMS

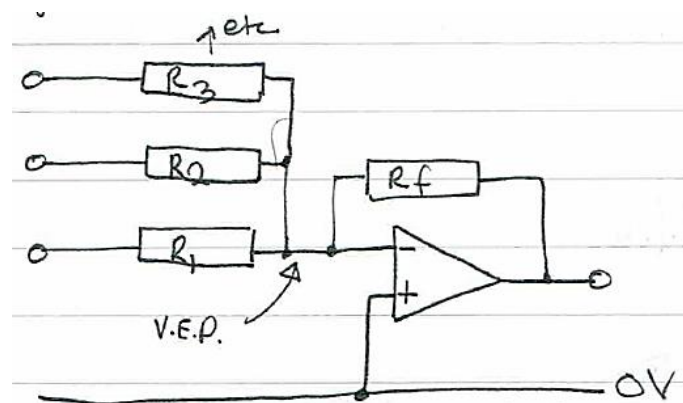
### Inverting amplifier



input resistance =  $R_{IN}$

$$G_V = -\frac{R_f}{R_{in}}$$

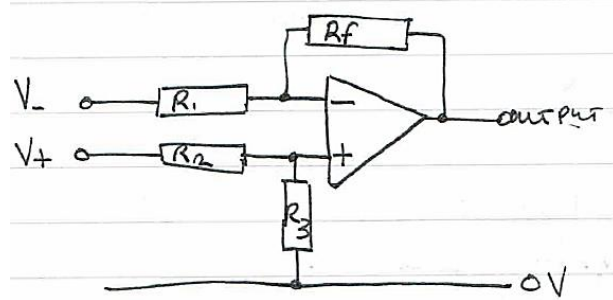
### Summing amplifier



input resistance = the relevant input resistor

$$V_{out} = -R_f \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

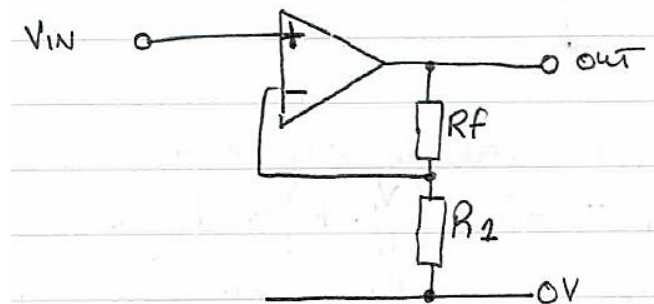
### Difference amplifier



$$V_{out} = \frac{R_f}{R_1} (V_+ - V_-)$$

- it is normal for  $R_1=R_2$  and  $R_3=R_f$  so as to match the small bias currents that pass into op-amp inputs
- applications: noise reduction in audio – send two inverted signal, subtract, giving greater signal while reducing the interference; similarly noise reduction in computer networks
- the input resistance is different at each input but is comparatively low.

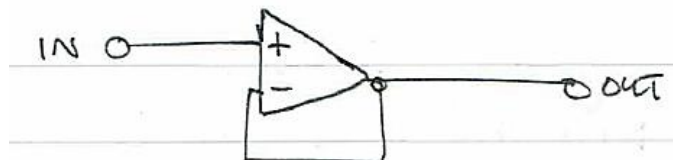
### Non-inverting amplifier



input directly into the op-amp, so input impedance = as that of the op-amp – as high as 10kΩ!

$$G_V = 1 + \frac{R_f}{R_1}$$

### The voltage follower (unity gain)



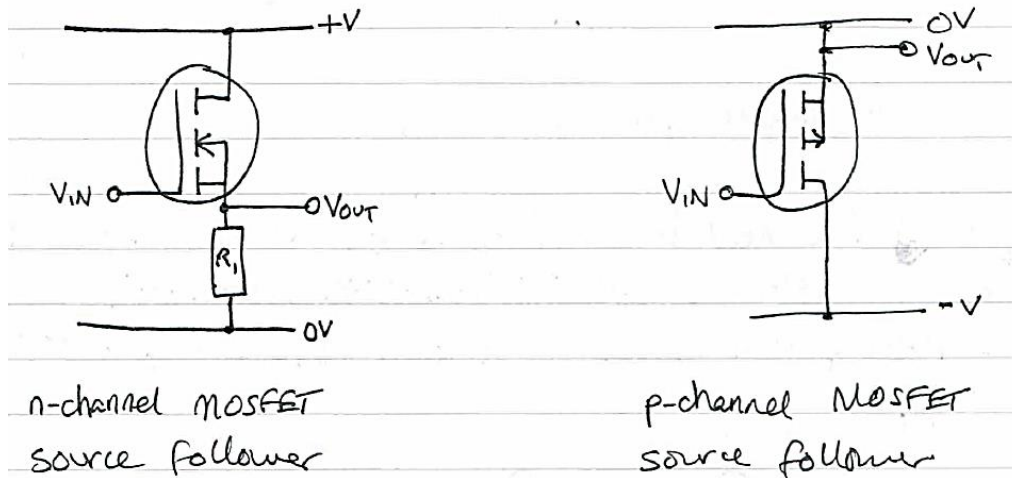
$$G_V = 1$$

- can be used as a 'buffer' to help avoid issues in a system – has considerable current and thus power gain, so can 'isolate' a source from a load. Very high input impedance and low output impedance.

## POWER AMPLIFIERS

bandwidth = range of frequencies over which  $G_p$  at least  $\frac{1}{2}$  max

### Source followers

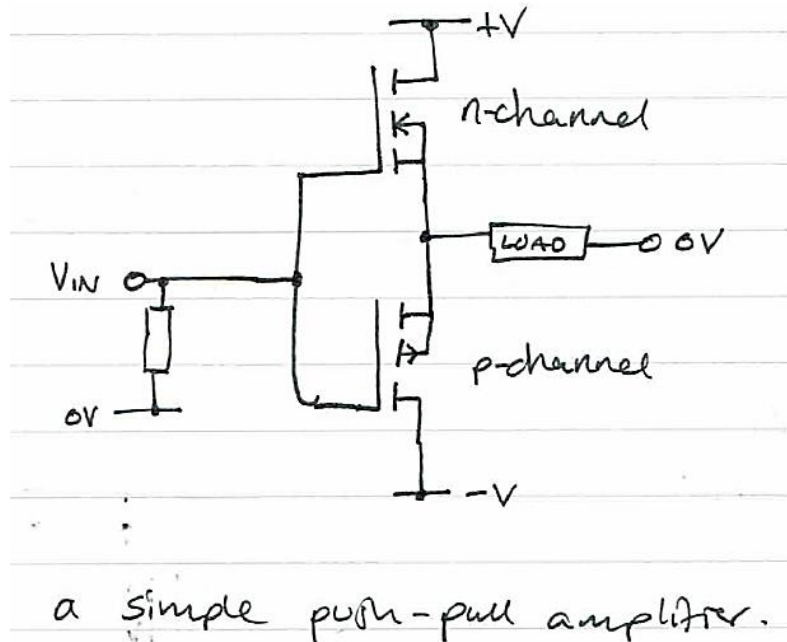


Applications include anywhere needing a unity gain amplifier / voltage buffer. The n-channel MOSFET handles positive voltage, and the p-channel negative voltage.

MOSFETs need a certain gate-source voltage before they will pass current – as much as 2V. This can lead to the output signal being distorted, but can be overcome by biasing them into conduction.

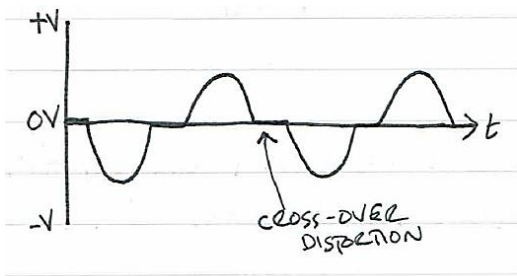
The power output of the source follower can be calculating using  $P = \frac{V^2}{R}$  where V is  $V_{RMS}$  and R is the load resistor, or  $P = IV$ , bearing in mind the current through the load must also pass through the MOSFET.

Push-pull amplifiers can handle both positive and negative voltages. Note that the two MOSFETs need to have matched characteristics.



Because of the need for a gate-source voltage, the output can be distorted, called “cross-over distortion.”

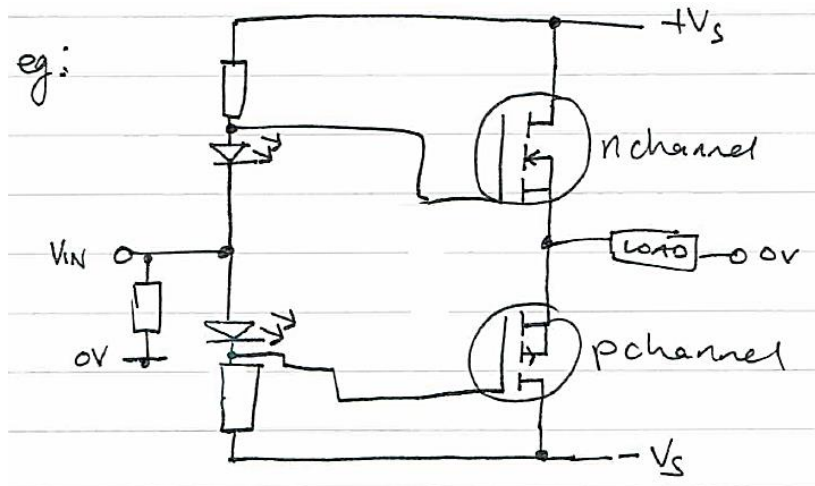
This push-pull amplifier has a much higher efficiency than the source follower – up to 90%.



To overcome crossover distortion, we need to bias the MOSFET so a small quiescent current flows even when there is no input signal. This reduces the effect of the distortion but does reduce efficiency to about 70%.

We can bias the MOSFETs using potential dividers or using LEDs (they have a similar 2V drop to that needed by the MOSFET), diodes, or a combination of both.

example of cross-over distortion. eg:



$$\text{for a push-pull amp, } P = \frac{V_s^2}{2R}$$

NB when buffering the output of an op-amp using the above, connect any feedback loop to the output of the MOSFET array (ie LOAD) rather than the start of it. This improves stability.

MOSFETs often need heatsinking to avoid thermal runaway. Do not heatsink multiple MOSFETs to the same conductive object as the heatsink tab is often connected to the drain and they will short circuit. Small insulators can be used combined with thermal paste if need be.